PATENT

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UTILITY PATENT APPLICATION TRANSMITTAL LETTER AND FEE TRANSMITTAL FORM (37 CFR 1.53(b))

BOX PATENT APPLICATION
Assistant Commissioner for Patents
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Sir:

Transmitted herewith for filing under 37 CFR 1.53(b) is:

☒ a patent application
☐ a Continuation ☐ a Divisional ☐ a Continuation-in-Part (CIP)
of prior application no.: ; filed .
☐ A Small Entity Statement(s) was filed in the prior application; Status still proper and desired.

Inventor(s) or Application Identifier:

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Kyungki-do, Republic of Korea

Entitled: OUTPUT-COMPENSATED BUFFER WITH SOURCE-FOLLOWER INPUT STRUCTURE AND IMAGE CAPTURE DEVICE USING SAME

Enclosed are:

1. ☒ Application Transmittal Letter and Fee Transmittal Form *(A duplicate is enclosed for fee processing)*
2. ☒ 14 pages of Specification (including 22 claims)
3. ☒ 7 sheets of Formal Drawings (35 USC 113)
4. ☒ Oath or Declaration
   a. ☒ newly executed *(original or copy)*
   b. ☐ copy from prior application (37 CFR 1.63(d) *(for continuation/divisional)* **[Note Box 5 Below]**
   c. ☐ DELETION OF INVENTOR(S) *(Signed statement deleting inventor(s) named in the prior application)*
5. ☐ Incorporation By Reference *(useable if box 4b is checked)*
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. ☐ Microfiche Computer Program *(Appendix)*
7. ☒ Assignment papers *(cover sheet(s) and document(s)*
8. ☐ Small Entity Statement(s)
9. ☐ Information Disclosure Statement, PTO-1449, and references cited
10. ☐ Preliminary Amendment ***(Please enter all claim amendments prior to calculating the filing fee.)***
11. ☐ English Translation Document
12. ☒ Certified Copy of Korean Appl. No. 98-39101 Filed September 21, 1999

13. ☐ Sequence Listing/ Sequence Listing Diskette
    a. ☐ computer readable copy
    b. ☐ paper copy
    c. ☐ statement in support
14. ☐ An Associate Power of Attorney
15. ☒ Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
16. ☐ Other:

The fee has been calculated as shown below:

	Column 1 No. Filed	Column 2 No. Extra	Small Entity Rate Fee	Large Entity Rate Fee
BASIC FEE			$380.00	$760.00
TOTAL CLAIMS	22 - 20 =	2	x 09 = $	x 18 = $36.00
INDEP CLAIMS	3 - 3 =	0	x 39 = $	x 78 = $0
☐ MULTIPLE Dependent Claims Presented			+ 130 = $	+ 260 = $
If the difference in Col. 1 is less than zero, Enter "0" in Col. 2			Total $	Total $796.00

☐ A check in the amount of $ to cover the filing fee is enclosed.

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☒ The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 50-0220.
- ☒ Any additional filing fees required under 37 CFR 1.16.
- ☒ Any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

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Candi L. Riggs
Date of Signature: September 20, 1999

Attorney Docket No. 5649-659

OUTPUT-COMPENSATED BUFFERS WITH SOURCE-FOLLOWER INPUT STRUCTURE, METHODS OF OPERATING SAME, AND IMAGE CAPTURE DEVICES USING SAME

Field of the Invention

The present invention relates to microelectronic devices, and more particularly, to signal buffers suitable for use in devices such as charged-coupled device (CCD) image capture systems.

Background of the Invention

Charge coupled devices (CCDs) are image capture devices that generally offer superior characteristics such as small size, light weight and low power consumption in comparison to other conventional image capture devices. Accordingly, CCDs are commonly used in broadcasting or domestic video cameras, monitoring cameras, and digital still cameras.

As manufacturing and designing techniques have progressed, the density of CCDs has generally increased, resulting in reduced size. As the size of CCDs has reduced, however, the levels of the signals produced by the image capture elements in CCDs have generally become smaller. Therefore, it has become desirable to use output buffers with high gain to produce signals usable for video processing and other purposes from such weak signals.

A typical output buffer is illustrated in FIG. 1. The output buffer includes an input source follower circuit including respective driving and load NMOS transistors **M1**, **M2** which are biased between a power supply voltage **VDD** and a signal ground. An input signal, e.g., a signal produced by a horizontal transfer section of a CCD image capture device, is applied to the gate terminal of the driving transistor **M1**, while a control signal **Vg** is applied to the gate terminal of the load transistor **M2**. A voltage produced on the source terminal of the driving transistor **M1** is generated responsive to the input signal **Vin**, and is applied to a second stage source follower circuit including driving and load transistors **M3** and **M4**. The second stage source

follower circuit similarly drives a third stage source follower circuit including driving and load transistors **M5**, **M6**, producing an output signal **Vout**. Achieving high gain from such a circuit can be problematic.

Summary of the Invention

In light of the foregoing, it is an object of the present invention to provide buffers with high-gain, suitable for use with devices such as CCD image capture devices.

It is another object of the present invention to provide buffers having source follower input circuits.

These and other objects, features and advantages may be provided according to the present invention by output-compensated buffers including a buffer circuit that includes a input source follower circuit, and a feedback circuit that variably capacitively couples a bias terminal of the input source follower to a power source, in response to the output of the buffer circuit. The feedback circuit is thus operative to vary the input capacitance of the buffer circuit responsive to the output signal. According to one embodiment of the present invention, the feedback circuit comprises another source follower circuit having an input that receives an output signal from the buffer circuit and an output that is capacitively coupled to the bias terminal of the input source follower circuit.

In particular, according to an embodiment of the present invention, an output-compensated buffer includes a buffer circuit that receives an input signal and produces an output signal responsive thereto at an output terminal, the buffer circuit including an input source-follower circuit that receives the input signal. A feedback circuit is connected to the output terminal and to the input source follower circuit and operative to vary an input capacitance of the source follower circuit responsive to the output signal at the output terminal. The input source follower circuit preferably comprises a bias terminal coupled to a power source, and the feedback circuit is preferably capacitively coupled to the bias terminal.

According to another embodiment of the present invention, the feedback transistor includes a first transistor having source terminal, a drain terminal connected to the power source, and a gate terminal connected to the output terminal of the buffer

circuit. The feedback circuit further includes a second transistor having a drain terminal connected to the source terminal of the first transistor at a signal node, a drain terminal connected to a signal ground and a gate terminal configured to receive a control signal. A capacitor is coupled between the signal node and the bias terminal of the source follower circuit.

According to another aspect of the present invention, an image capture device includes a charged coupled device (CCD) that generates a video signal. A buffer circuit is responsive to the CCD and operative to receive the video signal and produce an output signal responsive thereto at an output terminal, the buffer circuit including an input source-follower circuit that receives the video signal. A feedback circuit is connected to the output terminal and to the input source follower circuit and operative to vary an input capacitance of the source follower circuit responsive to the output signal at the output terminal.

Brief Description of the Drawings

FIG. 1 is a circuit diagram illustrating a conventional buffer with an input source follower circuit.

FIG. 2 is a circuit diagram illustrating a CCD in combination with an output-compensated buffer according to an embodiment of the present invention.

FIG. 3 is a circuit diagram illustrating an output-compensated buffer according to an embodiment of the present invention.

FIG. 4 is a circuit diagram illustrating an output-compensated buffer according to another embodiment of the present invention.

FIG. 5 is a circuit diagram of the output-compensate buffer of FIG. 4 in combination with a horizontal transfer section of a CCD.

FIGs. 6a-6b are waveform diagrams illustrating exemplary operations of an output-compensated buffer according to an embodiment of the present invention.

Detailed Description of Preferred Embodiments

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different

forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

FIG. 2 illustrates an image capture system **300** including a CCD image capture device **250** with a horizontal transfer section **200** and an output circuit including a reset transistor **120**, connected to an output-compensated buffer **140**, such as the output compensated buffers **140**, **140'** illustrated in FIGs. 3 and 4. The CCD image capture device **250** includes a P type semiconductor substrate **201** having a surface covered by an insulating layer **202**. A plurality of transfer gate electrodes **204** are formed on the insulating layer **202**. Electrodes **204** on an insulating layer **202** form an array and are driven by multi-phase clock signals (as shown, 3 phase clock signals $\phi 1$, $\phi 2$, $\phi 3$). An output electrode **206** is also formed on the insulating layer **202**.

An N type floating diffusion region **208** is formed on the substrate **201** near the output gate electrode **206**. A reset gate electrode **212** is formed on the insulating layer **202** near the floating diffusion region **208**, and another N type impurity region **210** is formed on the substrate **201** near the reset gate electrode **212** such that the reset gate electrode **212** is disposed between the floating diffusion region **208** and the N type impurity region **210**. As a result, a channel is formed beneath the reset gate electrode **212**, between the floating diffusion region **208** and the N type impurity region **210**. The floating diffusion region **208**, the N type impurity region **210** and the reset gate electrode **212** make up a reset transistor **120**.

The three clock signals $\phi 1$, $\phi 2$, $\phi 3$ are respectively applied to the transfer gate electrodes **204** such that a transfer well structure formed by the transfer gate electrodes **204** moves toward the output gate electrode **206**. The output gate electrode **206** receives gate signal **VOG**, while the reset gate electrode **212** receives reset signal

φR The N type impurity region **210** is biased to a drain voltage **VOD**. The signals **φ1**, **φ2**, **φ3**, **VOG**, **φR** are applied to the transfer gate electrodes **204**, the output gate electrode **206**, the reset gate electrode **212** and the N type impurity region **210** to control charge transfer to and from the floating diffusion region **208**. The floating diffusion region **208** is connected to the output-compensated buffer **140**, which buffers signals that are generated by transfer of charge to the floating diffusion region **208** by the action of the electrodes **204**, **206**, producing output signals (voltages) Vout.

In order to convert weak charges into signals, the output-compensated buffer **140** preferably exhibits high gain. In order to achieve such high gain, it is desirable to reduce and preferably minimize the capacitance at the diffusion region **208**, which includes the input capacitance of the output-compensated buffer **140**. For a charge injection of ΔQ, the variation ΔV in voltage at the diffusion region **208** is given by:

$$\Delta V = \frac{\Delta Q}{Cs},$$

where *Cs* indicates the capacitance at the diffusion region **208**. As can be seen in the above formula, reducing the capacitance C increases the voltage variation ΔV, and thus can improve sensitivity.

The relationship of capacitance of a signal source, such as the above described capacitance *Cs* of a CCD horizontal output section, connected to an input source follower circuit may be related to the input capacitance C of the input source follower circuit itself and the gain A1 of the input source follower circuit by:

$$C = (1 - A1)Cs,$$

where A1 has a value less than 1. As the input capacitance *C* of the input source follower circuit is decreased, the gain A1 is increased, thus resulting in increased gain for the output buffer in which the source follower circuit is used.

FIG. 3 illustrates an output-compensated buffer **140** according to an embodiment of the present invention. The output-compensated buffer **140** includes a

buffer circuit **7** and a feedback circuit **8**. The buffer circuit **8** includes an input terminal **2**, an output terminal **4**, a control terminal **6**, and a bias terminal **10**. As illustrated, the buffer circuit **8** includes a single source follower circuit including first and second NMOS transistors **M11** and **M12**. The first NMOS transistor **M11** has a gate terminal that receives an input signal **Vin** at the input terminal **2** and a source terminal connected to the drain terminal of the second NMOS transistor **M12**. The first NMOS transistor **M11** also has a drain terminal connected to a resistor **R1** at a node **N3**, with the resistor **R1** also being connected to a power source **VDD**, such that a secondary power supply voltage **VDD'** is applied to the drain terminal of the first NMOS transistor **M11**. The second NMOS transistor has a gate terminal that receives a control signal **Vg** applied at the control terminal **6** and a source terminal connected to a signal ground **GND**. In the source follower configuration shown, the first NMOS transistor **M11** serves as a driving transistor, while the second NMOS transistor **M21** serves as a load transistor.

The feedback circuit **8** includes another source follower circuit, including an NMOS transistor **M13** with a source terminal connected to a drain terminal of an NMOS transistor **M14** at a node **N2**. The NMOS transistor **M13** has a drain terminal connected to the power source **VDD**, and a gate terminal that receives the output signal **Vout** produced by the buffer circuit **7**. The NMOS transistor **M14** has a source terminal connected to the signal ground **GND** and a gate terminal that receives the control signal **Vg**. The node **N2** of the feedback circuit **8** is capacitively coupled to the node **N3** of the buffer circuit **7** by a capacitor **C1**. The capacitive coupling provided by the capacitor **C1** allows AC (alternating current) components to be transferred to the power source **VDD**, which reduces the input capacitance of the NMOS transistor **M11** of the buffer circuit through a Miller effect. This can increase the AC gain of the output-compensated buffer **140**.

FIG. 4 illustrates an output compensated buffer **140'** according to another embodiment of the present invention. The output-compensated buffer **140'** includes a buffer circuit **7'** with an input terminal **2'**, an output terminal **4'**, a control terminal **6'** and a bias terminal **10'**. The buffer circuit **7'** has a 3-stage structure including an input source follower circuit **14** and additional second and third stage source follower circuits **10**, **12**. The input source follower circuit **14** includes driving and load NMOS

transistors **M21**, **M22**. A gate terminal of the driving transistor **M21** receives an input signal **Vin** applied at the input terminal **2'**, and has a source terminal connected to the drain terminal of the load transistor **M22**. The gate terminal of the load transistor **M22** receives a control signal **Vg** applied at the control input **6'**. The drain terminal of the driving transistor is connected to one terminal of a resistor **R2** at a node **N4**. The resistor **R2** has a second terminal connected at to a power source **VDD**, such that a secondary power supply voltage **VDD'** is applied to the drain terminal of the driving transistor **M21**.

The second and third stage source follower circuits **12**, **10** include respective driving/load transistor pairs **M19/M20**, **M17/M18**. The gate terminal of the driving transistor **M19** of the second stage source follower circuit **12** is connected to the output of the input source follower circuit **14**, i.e., at the junction of the source and drain terminals of the driving and load transistors **M21**, **M22**. The drain terminal of the driving transistor **M19** is connected to the power source **VDD**. The gate terminal of the driving transistor **M17** of the third stage source follower circuit **10** is connected to the output of the second stage source follower circuit **12**, at the junction of the source and drain terminals of the driving and load transistors **M19**, **M20**. The drain terminal of the driving transistor **M17** is connected to the power source **VDD**. The output of the third stage source follower circuit, i.e., the junction of the source and drain terminals of the driving and load transistors **M17**, **M18**, is connected to the output terminal **4'**, where the output signal **Vout** is produced.

The output compensated buffer **140'** is connected to a feedback circuit **8** such as previously described with reference to FIG. 3. The capacitor **C1** of the feedback circuit **8** is connected to the first source follower circuit **14** and the gate of the transistor **M13** of the feedback circuit **8** is connected to the output of the third source follower circuit **10**. As the components of the feedback circuit **8** have been described with reference to FIG. 3, they will not be discussed in further detail.

FIG. 5 is a schematic diagram illustrating the output-compensated buffer **140'** of Fig. 4 in combination with a CCD horizontal transfer section **200** and reset transistor **120**. Charges supplied by the horizontal transfer section **200** are injected at the source terminal of the reset transistor **120**. The voltage Vin at the source terminal of the reset transistor **120** is applied to the input source follower circuit **14** of the

buffer circuit **7'**. As the components of the output buffer circuit **140'** have been previously described with reference to FIG. 4, further detailed description of these components will not be provided.

Referring to FIG. 6a, as the level of the input signal **Vin** increases, the voltage at the source terminal of the driving transistor **M21** increases proportionally to the input signal **Vin**. The voltage levels produced at the source terminals of the driving transistors **M19** and **M17** of the second and third stage source follower circuits **12** and **10** also increase proportionally to the voltages applied to their respective gate terminals, producing an output signal **Vout** that increases responsive to an increase in the input signal **Vin**. As shown in FIG. 6b, the AC gain of the buffer circuit is boosted by the action of the capacitor **C1** and the feedback circuit **8**, by boosting the effective bias voltage (secondary power supply voltage) **VDD'** applied the drain terminal of the driving transistor **M21**.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

THAT WHICH IS CLAIMED IS:

1. An output-compensated buffer, comprising:

a buffer circuit that receives an input signal and produces an output signal responsive thereto at an output terminal, said buffer circuit including an input source-follower circuit that receives the input signal; and

a feedback circuit connected to said output terminal and to said input source follower circuit and operative to vary an input capacitance of said source follower circuit responsive to the output signal at said output terminal.

2. An output-compensated buffer according to Claim 1:

wherein said input source follower circuit comprises a bias terminal coupled to a power source; and

wherein said feedback circuit is coupled to said bias terminal.

3. An output-compensated buffer according to Claim 2, wherein said feedback circuit is capacitively coupled to said bias terminal.

4. An output-compensated buffer according to Claim 3, wherein said feedback circuit is operative to variably capacitively couple the bias terminal to the power source responsive to the output signal at the output terminal.

5. An output-compensated buffer according to Claim 4, wherein said feedback circuit comprises a second source follower circuit having an input terminal that receives the output signal from the input source follower circuit of the buffer circuit and an output terminal capacitively coupled to the bias terminal of the input source follower circuit.

6. An output-compensated buffer according to Claim 5, wherein said second source follower circuit comprises:

a first transistor having source terminal, a drain terminal connected to the power source, and a gate terminal connected to the output terminal of the buffer circuit;

a second transistor having a drain terminal connected to the source terminal of the first transistor at a signal node, a drain terminal connected to a signal ground and a gate terminal configured to receive a control signal; and

a capacitor coupled between the signal node and the bias terminal of the source follower circuit.

7. An output-compensated buffer according to Claim 2:

wherein said source follower circuit comprises:

a first transistor having a source terminal, a gate terminal configured to receive the input signal, and a drain terminal connected to the power source through the resistor; and

a second transistor having a drain terminal connected to the source terminal of the first transistor, a source terminal connected to a signal ground and a gate terminal configured to receive a control signal; and

wherein said feedback circuit is coupled to the drain terminal of said first transistor.

8. An output-compensated buffer according to Claim 7, wherein said feedback circuit is capacitively coupled to the drain terminal of the first transistor.

9. An output-compensated buffer according to Claim 8, wherein said feedback circuit is operative to variably capacitively couple the drain terminal of the first transistor to the power source responsive to the output signal at the output terminal.

10. An output-compensated buffer according to Claim 9, wherein said feedback circuit comprises:

a third transistor having source terminal, a drain terminal connected to the power source, and a gate terminal connected to the output terminal of the buffer circuit;

a fourth transistor having a drain terminal connected to the source terminal of the third transistor, a drain terminal connected to a signal ground and a gate terminal configured to receive a control signal; and

a capacitor coupled between the drain terminal of the fourth transistor and the drain terminal of the first transistor.

11. An output-compensated buffer according to Claim 2, wherein the output terminal of the buffer circuit is an output terminal of the source follower circuit.

12. An output-compensated buffer according to Claim 2, wherein the buffer circuit further comprises a second source follower circuit connected to an output of the input source follower circuit and operative to produce the output signal responsive to the input signal applied to the input source follower circuit.

13. An output-compensated buffer according to Claim 1, in combination with a CCD image capture device, wherein the CCD image capture device includes a horizontal transfer section that generates the input signal.

14. An output-compensated buffer, comprising:

a buffer circuit that receives an input signal and produces an output signal responsive thereto at an output terminal, said buffer circuit including an input source-follower circuit that has an input terminal that receives the input signal and a bias terminal that receives a bias voltage from a power source; and

a feedback circuit connected to said output terminal and to said input source follower circuit and operative to variably couple the power source and the bias terminal via a capacitor.

15. An output-compensated buffer according to Claim 14:

wherein said source follower circuit comprises:

a first transistor having a source terminal, a gate terminal configured to receive the input signal, and a drain terminal connected to the power source through the resistor; and

a second transistor having a drain terminal connected to the source terminal of the first transistor, a source terminal connected to a signal ground and a gate terminal configured to receive a control signal; and

wherein said feedback circuit is coupled to the drain terminal of said first transistor.

16. An output-compensated buffer according to Claim 15, wherein said feedback circuit comprises:

a third transistor having source terminal, a drain terminal connected to the power source, and a gate terminal connected to the output terminal of the buffer circuit;

a fourth transistor having a drain terminal connected to the source terminal of the third transistor, a drain terminal connected to a signal ground and a gate terminal configured to receive a control signal; and

a capacitor coupled between the drain terminal of the fourth transistor and the drain terminal of the first transistor.

17. An output-compensated buffer according to Claim 14, wherein the output terminal of the buffer circuit is an output terminal of the source follower circuit.

18. An output-compensated buffer according to Claim 13, wherein the buffer circuit further comprises a source follower circuit connected to an output of the input source follower circuit and operative to produce the output signal responsive to the input signal applied to the input source follower circuit.

19. An output-compensated buffer according to Claim 14 in combination with a CCD image capture device, wherein the CCD image capture device comprises a horizontal transfer section that generates input signal.

20. An image capture device, comprising:

a charged coupled device (CCD) that generates a video signal;

a buffer circuit responsive to the CCD and operative to receives the video signal and produce an output signal responsive thereto at an output terminal, said buffer circuit including an input source-follower circuit that receives the video signal; and

a feedback circuit connected to said output terminal and to said input source follower circuit and operative to vary an input capacitance of said source follower circuit responsive to the output signal at said output terminal.

21. A image capture device according to Claim 20:

wherein said input source follower circuit comprises a bias terminal coupled to a power source; and

wherein said feedback circuit is coupled to said bias terminal.

22. An image capture device according to Claim 20, wherein said feedback circuit is operative to variably capacitively couple the bias terminal to the power source responsive to the output signal at the output terminal.

OUTPUT-COMPENSATED BUFFERS WITH SOURCE-FOLLOWER INPUT STRUCTURE, METHODS OF OPERATING SAME, AND IMAGE CAPTURE DEVICES USING SAME

Abstract of the Disclosure

An output-compensated buffer includes a buffer circuit that receives an input signal and produces an output signal responsive thereto at an output terminal, the buffer circuit including an input source-follower circuit that receives the input signal. A feedback circuit is connected to the output terminal and to the input source follower circuit and operative to vary an input capacitance of the source follower circuit responsive to the output signal at the output terminal. The input source follower circuit preferably comprises a bias terminal coupled to a power source, and the feedback circuit is preferably capacitively coupled to the bias terminal. According to another aspect, an image capture device includes a charged coupled device (CCD) that generates a video signal. A buffer circuit is responsive to the CCD and operative to receives the video signal and produce an output signal responsive thereto at an output terminal, the buffer circuit including an input source-follower circuit that receives the video signal. A feedback circuit is connected to the output terminal and to the input source follower circuit and operative to vary an input capacitance of the source follower circuit responsive to the output signal at the output terminal.

Fig. 1

(Prior Art)

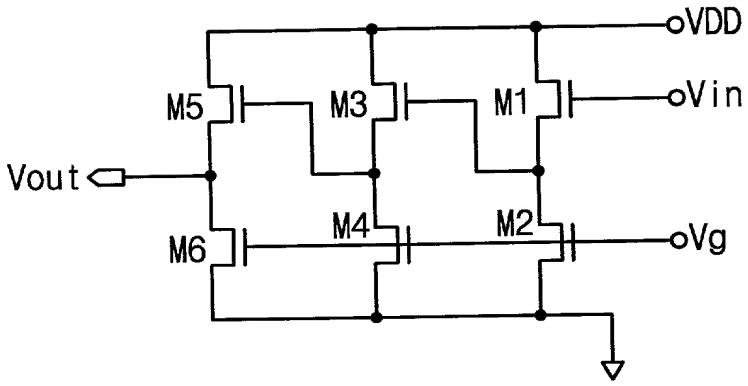


Fig. 2

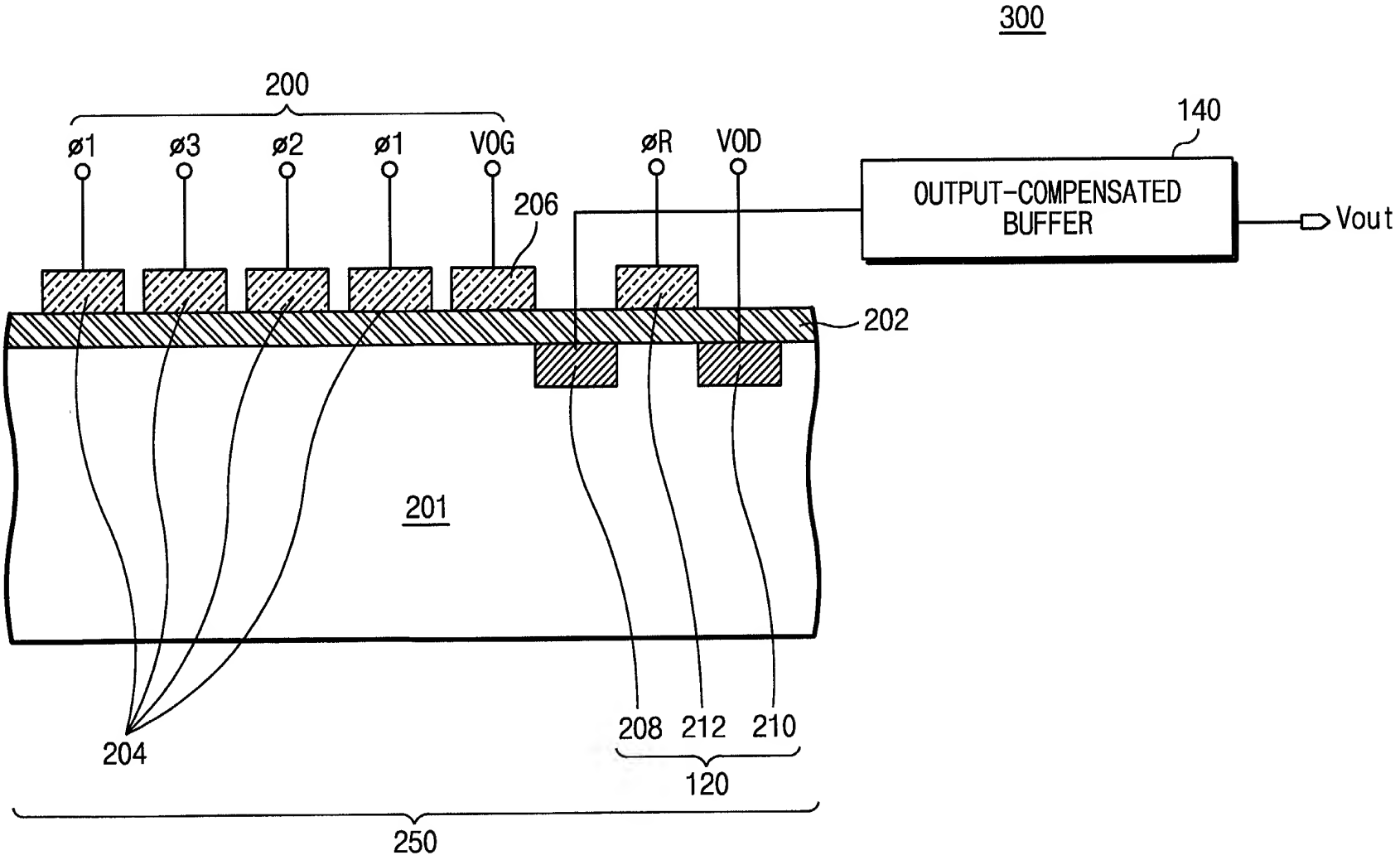

300
200
ø1
ø3
ø2
ø1
VOG
øR
VOD
140
OUTPUT-COMPENSATED BUFFER
Vout
206
202
201
204
208
212
210
120
250

Fig. 3

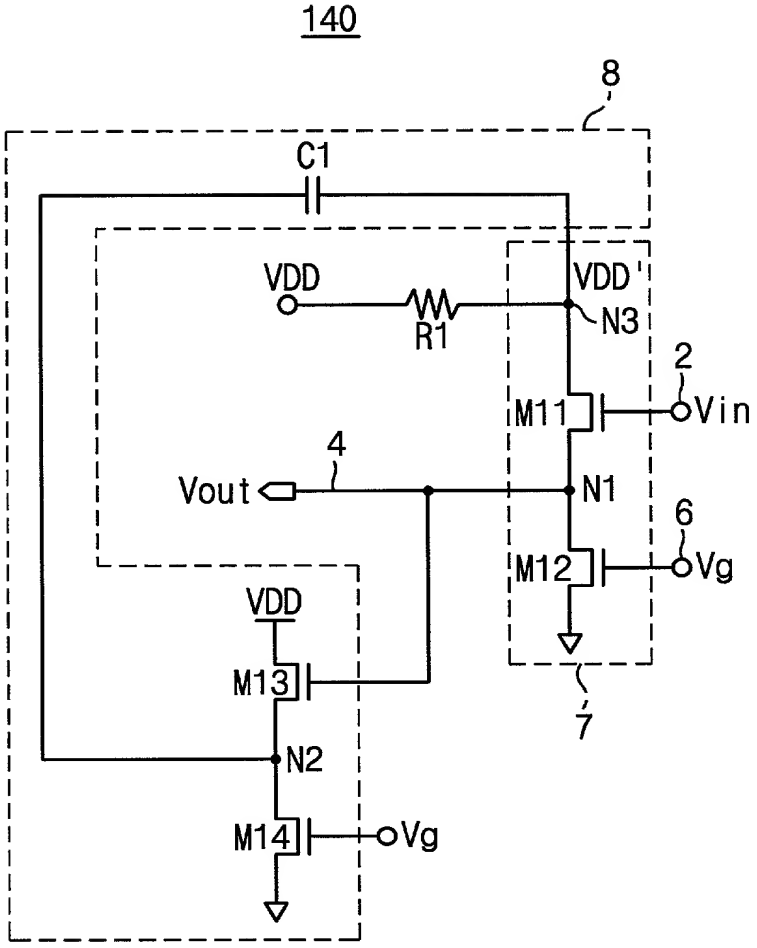

140
8
C1
VDD
R1
VDD'
N3
2
M11
Vin
4
Vout
N1
6
M12
Vg
VDD
M13
7
N2
M14
Vg

Fig. 4

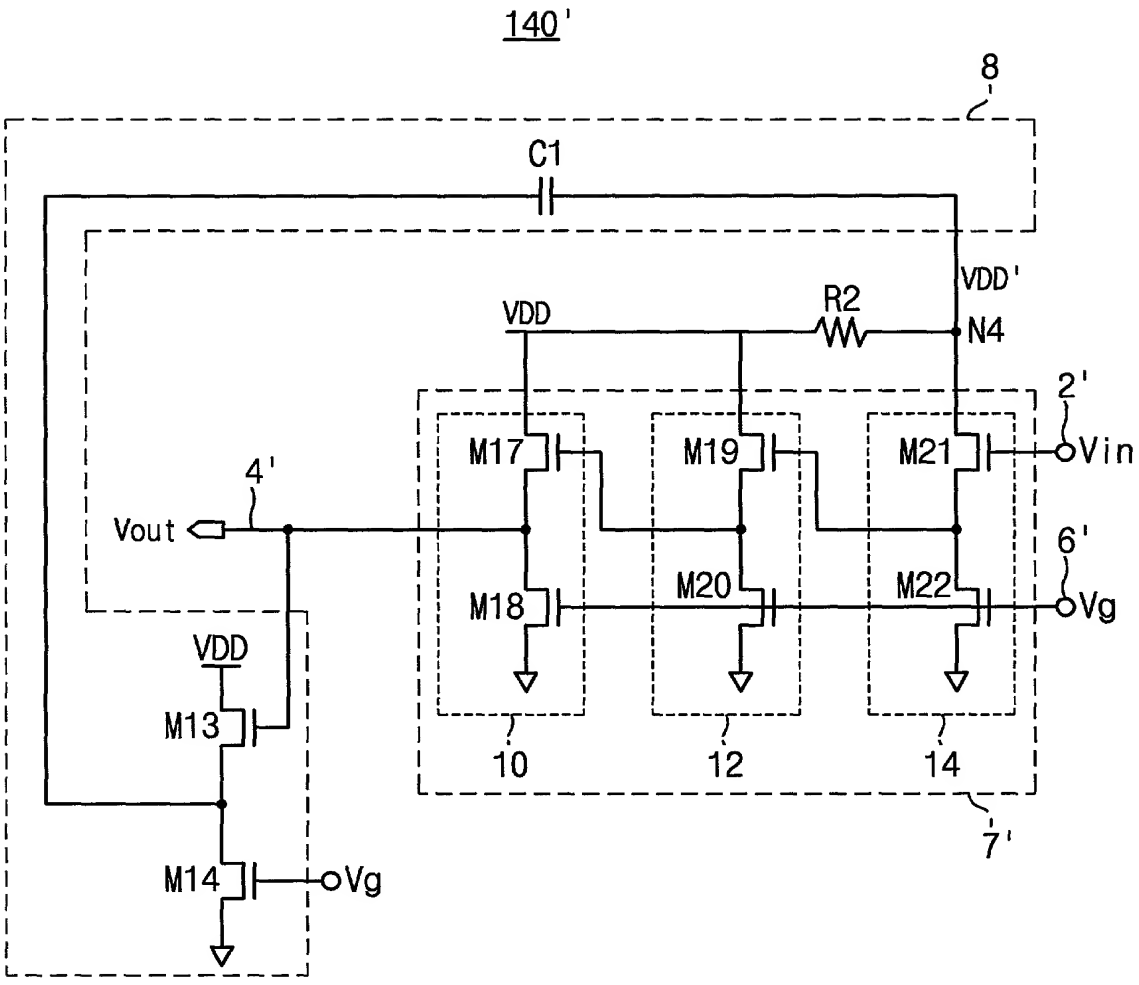

140'
8'
C1
VDD'
VDD
R2
N4
2'
Vin
M17
M19
M21
4'
Vout
6'
M18
M20
M22
Vg
VDD
M13
10
12
14
7'
M14
Vg

Fig. 5

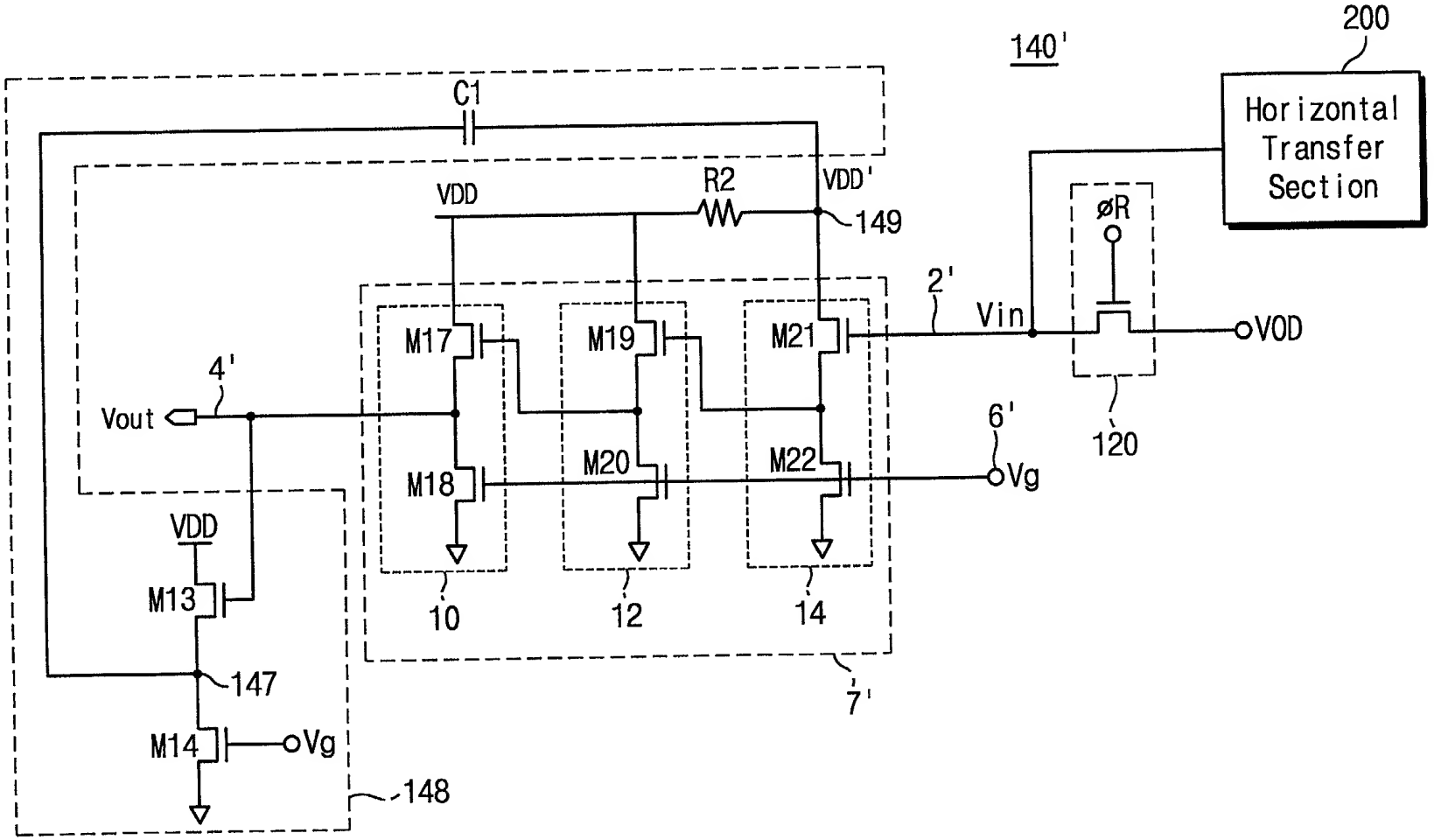

200
140'
Horizontal Transfer Section
C1
VDD
R2
VDD'
149
øR
2'
Vin
VOD
M17
M19
M21
4'
Vout
6'
M18
M20
M22
Vg
120
VDD
M13
10
12
14
147
M14
Vg
148
7'

Fig. 6a

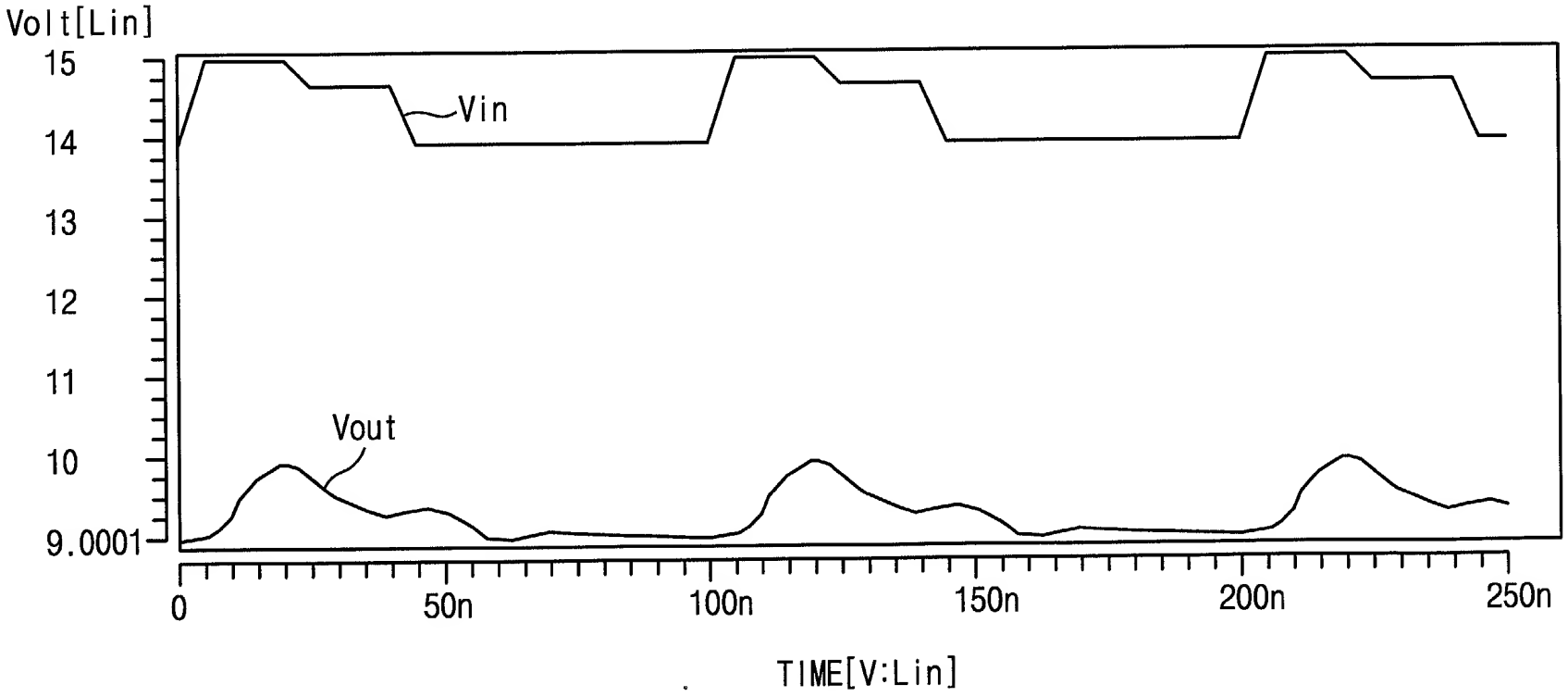
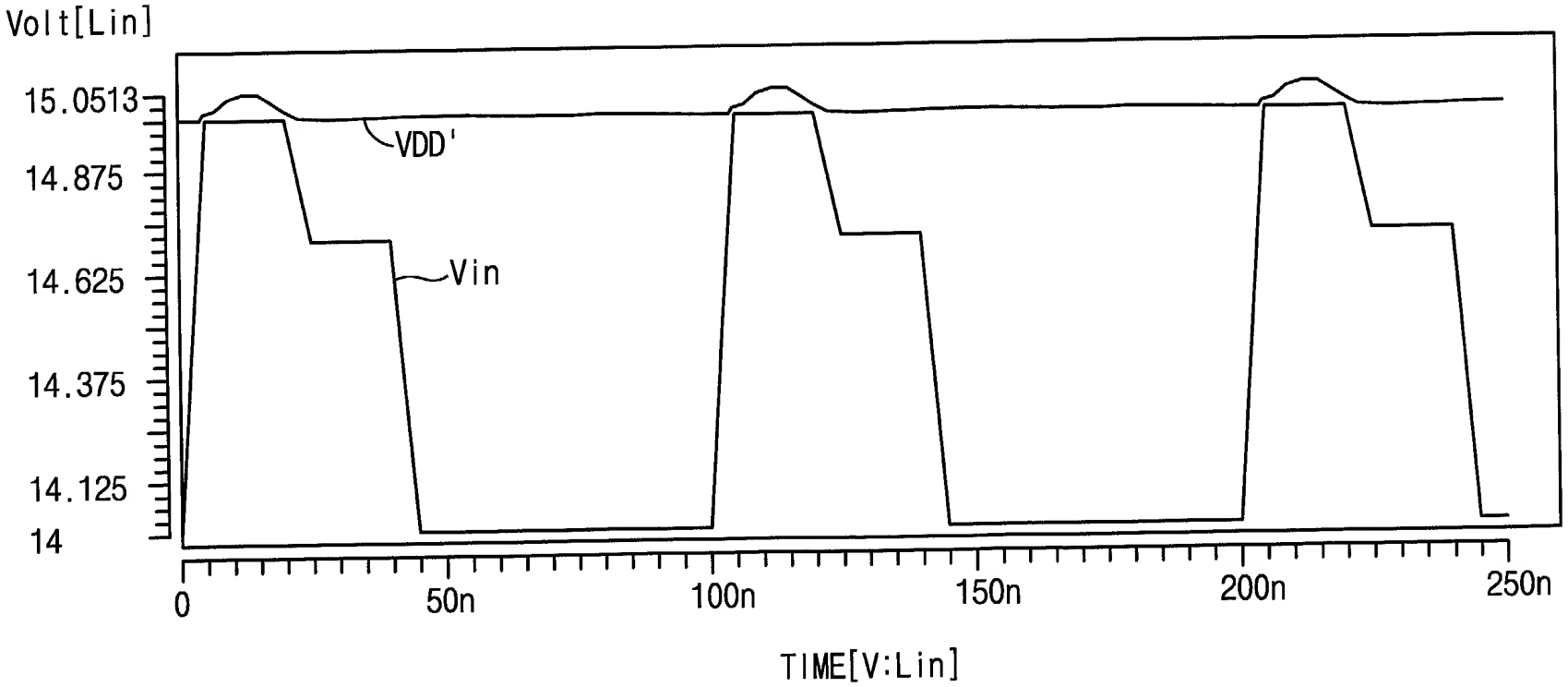

Volt[Lin]
15
14
13
12
11
10
9.0001
Vin
Vout
0
50n
100n
150n
200n
250n
TIME[V:Lin]

Fig. 6b


Volt[Lin]
15.0513
14.875
14.625
14.375
14.125
14
VDD'
Vin
0
50n
100n
150n
200n
250n
TIME[V:Lin]

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

Attorney Docket No. 5649-659

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **OUTPUT-COMPENSATED BUFFER WITH SOURCE-FOLLOWER INPUT STRUCTURE AND IMAGE CAPTURE DEVICE USING SAME.**

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate, or of any PCT International application having a filing date before that of the application on which priority is claimed.

98-39101	Korea	09/21/1998	[X] Yes [ ] No
Number	Country	MM/DD/YYYY Filed	Priority Claimed
			[ ] Yes [ ] No
Number	Country	MM/DD/YYYY Filed	Priority Claimed
			[ ] Yes [ ] No
Number	Country	MM/DD/YYYY Filed	Priority Claimed

ENGLISH LANGUAGE DECLARATION CONTINUED

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following registered attorney(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Customer Number 20792

I hereby authorize the above-named attorneys to accept and follow instructions from my Korean or United States representatives, Samsung Electronics, as to any action to be taken in the U.S. Patent and Trademark Office regarding this application without direct communication between the above-named attorneys and myself. In the event of a change in the persons from whom instructions may be taken, I will notify the above-named attorneys.

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